

**Assembly Relocation to STATS ChipPAC Jiangyin
and Test Transfer to STATS ChipPAC Singapore of Select QFP Products**

**Automotive Qualification Plan Summary for
LQFP at STATS ChipPAC China Jiangyin**

TEST	SPECIFICATION	SAMPLE SIZE	EXPECTED COMPLETION DATE
Temperature Cycle (TC)*	JEDEC <i>JESD22-A104</i>	3 x 77	June 2016
Solder Heat Resistance (SHR)*	JEDEC/IPC <i>J-STD-020</i>	3 x 11	June 2016
Highly Accelerated Stress Test (HAST)*	JEDEC <i>JESD22-A110</i>	3 x 77	June 2016
Unbiased Highly Accelerated Stress Test (uHAST)*	JEDEC <i>JESD22-A118</i>	3 x 77	June 2016
High Temperature Storage (HTS)	JEDEC <i>JESD22-A103</i>	1 x 77	June 2016
Electrostatic Discharge <i>Field Induced Charge Device Model</i>	JEDEC <i>JESD22-C101</i>	3/voltage	June 2016

* These samples will be subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: 1. Bake – 24 hours at 125°C; 2. Soak – unbiased soak for 192 hours at 30°C, 60%RH; 3. Reflow – three passes through a reflow oven with a peak temperature of 260°C. TC samples will be subjected to wire-pull test after 500 cycles where results should be within specification limits.

**Assembly Relocation to STATS ChipPAC Jiangyin and
Test Transfer to STATS ChipPAC Singapore of Select QFP Products**

**Automotive Qualification Plan Summary for LQFP_EP and
MQFP at STATS ChipPAC China Jiangyin**

TEST	SPECIFICATION	SAMPLE SIZE	EXPECTED COMPLETION DATE
Temperature Cycle (TC)*	JEDEC <i>JESD22-A104</i>	3 x 32	June 2016
Solder Heat Resistance (SHR)*	JEDEC/IPC <i>J-STD-020</i>	3 x 11	June 2016
Highly Accelerated Stress Test (HAST)*	JEDEC <i>JESD22-A110</i>	3 x 32	June 2016
Unbiased Highly Accelerated Stress Test (uHAST)*	JEDEC <i>JESD22-A118</i>	3 x 32	June 2016
High Temperature Storage (HTS)	JEDEC <i>JESD22-A103</i>	1 x 32	June 2016
Electrostatic Discharge <i>Field Induced Charge Device Model</i>	JEDEC <i>JESD22-C101</i>	3/voltage	June 2016

* These samples will be subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: 1. Bake – 24 hours at 125°C; 2. Soak – unbiased soak for 192 hours at 30°C, 60%RH; 3. Reflow – three passes through a reflow oven with a peak temperature of 260°C. TC samples will be subjected to wire-pull test after 500 cycles where results should be within specification limits.

**Assembly Relocation to STATS ChipPAC Jiangyin and
Test Transfer to STATS ChipPAC Singapore OF Select QFP Products**

**Qualification Plan Summary for TQFP and TQFP_EP
at STATS ChipPAC China Jiangyin**

TEST	SPECIFICATION	SAMPLE SIZE	EXPECTED COMPLETION DATE
Temperature Cycle (TC)*	JEDEC <i>JESD22-A104</i>	3 x 32	April 2016
Solder Heat Resistance (SHR)*	JEDEC/IPC <i>J-STD-020</i>	3 x 11	April 2016
Unbiased Highly Accelerated Stress Test (uHAST)*	JEDEC <i>JESD22-A118</i>	3 x 32	April 2016
Electrostatic Discharge <i>Field Induced Charge Device Model</i>	JEDEC <i>JESD22-C101</i>	3/voltage	April 2016

* Preconditioned per JEDEC/IPC J-STD0020

Test Correlation Plan

1. SCC Correlation Data Gathering

- Loop 4 bin1 units x30
- Run 100 bin1 units on handler
- Serialize and test 10 bin1 units
- Serialize and test 5 reject units

2. Ship correlation package from SCC to STA

3. STA Correlation Data Gathering

- Loop 4 bin1 units x30
- Run 100 bin1 units on handler
- Test 10 already serialized bin1
- Test 5 already serialized rejects

4. SCC send data to ADGT for Data Crunching and Analysis

5. CorL8 Analysis of x30 loop /100 units handler data

- X30 loop must pass Mean Shift, Sigma Spread and CPK criteria
- 100 Bin1 Correlation units must pass Mean Shift, Sigma Spread and CPK criteria
- 10 serialized units must pass bin1 both in SCC and in STA
- 5 serialized rejects must fail the same parameter for both SCC and STA

6. Correlation Data Approval

- For TRB movement to Available with Condition

7. Validation lot run handled by STA

Note: CorL8 is ADI data analysis tool.

Correlation Test Criteria(TST00137)

% Mean Shift Criteria	$((SCC_mean - STA_Mean) / (Upper_Limit - Lower_Limit)) \times 100 \leq 5$
Sigma Spread Criteria	$(STA_Sigma / SCC_Sigma) \leq 1.300000$
Cpk Criteria	If CPK to the test limits is >10, then test given automatically PASS

Reject Correlation



Unit	SCC	STA
1	TnumX: XXXXX	TnumX: XXXXX
...	TnumX: XXXXX	TnumX: XXXXX
5	TnumX: XXXXX	TnumX: XXXXX

Bin1 Correlation

Unit	SCC	STA
1	Pass	Pass
...	Pass	Pass
10	Pass	Pass

Test Correlation Estimated Timeline

Devices	Dec, 2015 to June, 2016	Dec, 2015 to August 2016	September, 2016
SCC Correlation Data Gathering & Shipment	PLANNED	PLANNED	
SCS Correlation Data Gathering		PLANNED	
Data Review and Approved by ADGT		PLANNED	
Validation Run/TRB Closure		PLANNED	PLANNED

 PLANNED
 ACTUAL/ADJUSTED